calorimeter. There are eight rear mounted Receiver cards, eight front mounted Electron Isolation cards, and one front mounted Jet Summary card for a total of 17 cards per crate dedicated to processing data from the calorimeter.

3. Receiver Card

The Receiver card is the largest board in the crate. It is 9U by 400mm. The rear side of the card receives the calorimeter data from optical fibers, translates from fibre to copper, and converts from serial to parallel format. The front side of the card contains circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. There are also lookup tables and adder blocks on the front. The lookup tables translate the incoming information to transverse energy on several scales. They are also used to test for Quiet and Minimum Ionization thresholds for each trigger tower. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for intercrate sharing.

Each card is designed to receive 32 fibres from the FERMI [2] front-end readout system on the calorimeter. Each fibre transmits either two towers of hadronic or electromagnetic information per crossing. The data is transmitted on the fiber in a compressed eight bit format, providing a total of 16 data bits. The present design uses transmitter and receiver links capable of handling 21 bits of information in 25 nsec with a baud rate of 960 Mbaud. The additional 5 bits, not used for data, contain a single Hamming code generated from the 16 bits of data. This code is sufficient to detect all single and double bit errors as well as many multiple bit errors.

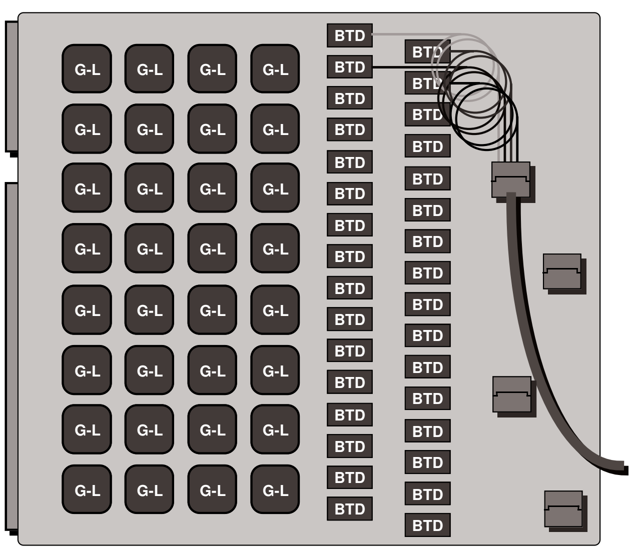

Figure 3. Rear view of the Receiver card.

The rear of the Receiver card is shown in Figure 3. The fibre receiver is made up of two separate components: The fibre to copper converter and the serial to parallel converter. As optical communication technology advances it is possible that integrated receivers (fibre to copper/serial to parallel), suitable to our application, will become available. Two separate fibre receivers have been considered for this design. The first device, made by BT&D, is a high quality component in a 24 pin package, with long laser diode lifetime (transmitter), and a fiber pigtail. The second converter is a more recent offering by Finisar. It is designed to handle data rates over the range of 100 Mbaud to 1.5 Gbaud and drive fibre lengths up to 500 M.The second component of the receiver duo is the serial to parallel converter. For the present design we have considered the Hewlett Packard HDMP-1014.

Figure 4 shows the synchronization circuitry contained on the front side of the Receiver card along with the memory look up tables and adder tree. The outputs of the HP receivers are not only unsychronized with the local clock but are also not aligned to the same bunch crossing. The synchronization circuitry is contained on an ASIC (Synchronization ASIC) that follows a concept originally proposed to handle the SDC fiber link word synchronization [2] .

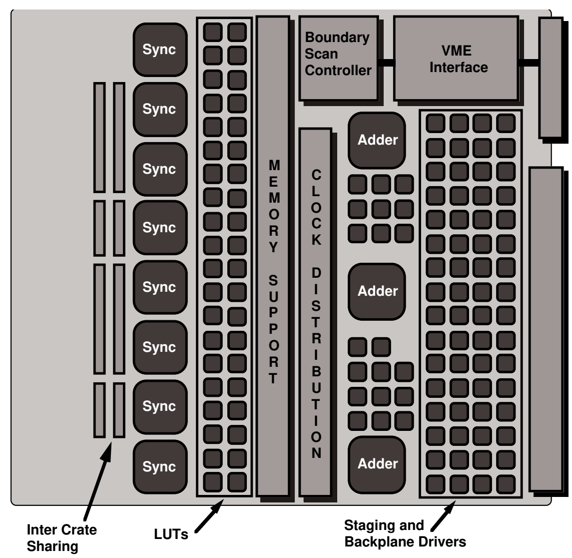

Figure 4. Front view of the Receiver card

In order to achieve maximum utilization of board space, all the logic following and including the Synchronization ASIC is run at 160 MHz. There are also four Error Correcting Codes (ECCs) associated with the four input channels. After synchronization, each is checked against the data. If an error is detected a single bit is set, one for each incoming channel, and appended to the original ECC code.

Lookup tables are required to translate the information coming from the calorimeter front end electronics, in compressed format, onto the several different scales used by the energy adder tree and the Electron Isolation logic. The Hadronic and Electromagnetic energies are individually translated into eight bits of linear E_T with a resolution of

[2] M.A. Thompson. SDC Link Word Synchronization, SDC Note SDC-93-536

approximately one GeV. These values are summed to provide total energy in 4 x 4 trigger tower regions of the calorimeter.

The transverse energy for each of the two 4 x 4 trigger tower regions is independently summed and forwarded to the Jet Summary card. On the Jet Summary card these E_T sums are used to continue the energy summation tree and also compared against a threshold to determine whether any sub-region contained jets. The E_T sums are applied to a set of lookup tables to generate E_X and E_Y for each 4 x 4 region. A separate adder tree is used to sum up E_X and E_Y from the regional values.

Though the input values at the top of the adder tree have only 8 bits of range, the adder tree has been designed to handle a dynamic range of 10 bits for either positive or negative values. This implies an overflow at approximately 1000 GeV, using the compressed scale described in the CMS Level 1 Calorimeter Trigger Performance Studies [3] .

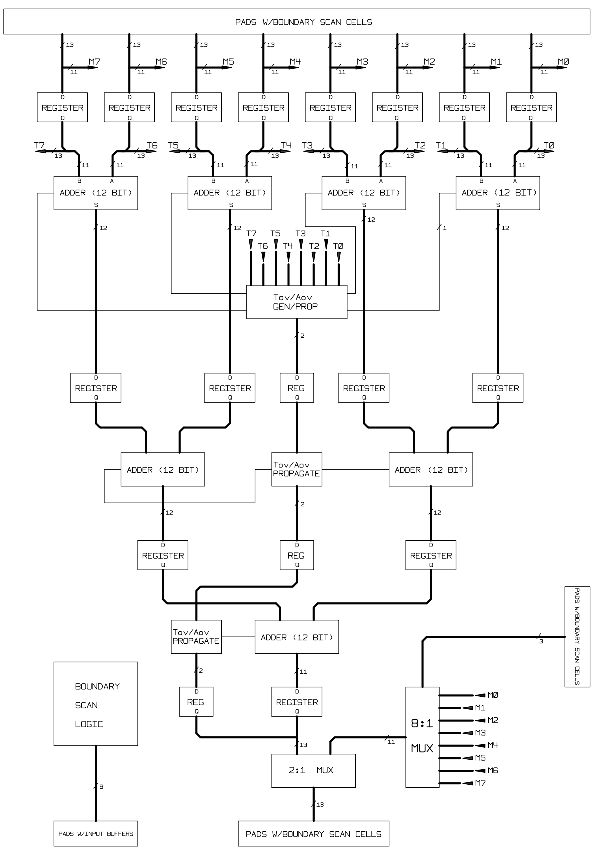

Figure 5. Block diagram of the Adder ASIC.

The adder ASIC is implemented as a 4-stage pipeline with eight input operands and 1 output operand. There are only three stages of adder tree, but an extra level of storage has been added to ensure chip processing is isolated from the I/O. We have determined that the ASIC must work reliably at a clock period of 5.0 nsec in order to ensure safe operation at an in-

[3] S. Dasu et al. CMS Level 1 Calorimeter Trigger Performance Studies, CMS TN/94-285 (1994)

circuit period of 6.25 nsec. The adder tree is composed of 4 bit adder macro cells to implement twelve bit wide adders. Eleven bits are wired, left justified, to each operand of an adder. The LSB of each adder will be internally set to ZERO. The MSB is treated as a sign bit. Therefore, although the adder tree may be constructed from three 4 bit adders, the width of the operand data paths has been limited to eleven bits.

The top of the adder tree is composed of four 12 bit adders and includes the logic required to detect and pass along overflows. Edge triggered registers are used to store the results for the next stage of the adder tree. A block diagram of the Adder ASIC is shown in Figure 5. The second stage contains two more 12 bit adders and includes the logic needed to propagate and detect overflows. Edge triggered registers are used to store the results for the next stage of the adder tree. The third stage contains the final adder as well as a continuation of the overflow circuitry. The register at this level is the last storage element before the ASIC output. We retain the identity of the tower overflow bits through the entire tree.

The ASIC has been produced by Vitesse in 0.6 µ H-GaAs, consists of approxiomately 11,000 cells, uses 4 W, has been simulated to function at 308 MHz and tested to 200 MHz, considerably above the 160 MHz requirement.

4. Electron Isolation Card

The Electron Isolation Card, shown in figure 6, receives data at 160 MHz in a staged fashion from at most nine Receiver Cards and performs the isolated electron algorithm described in the introduction. Some of the data originates from Receiver cards in neighboring crates, but is transmitted through the local Receiver cards. The Electron Isolation card is 9U x 280mm and resides in the front of the crate.

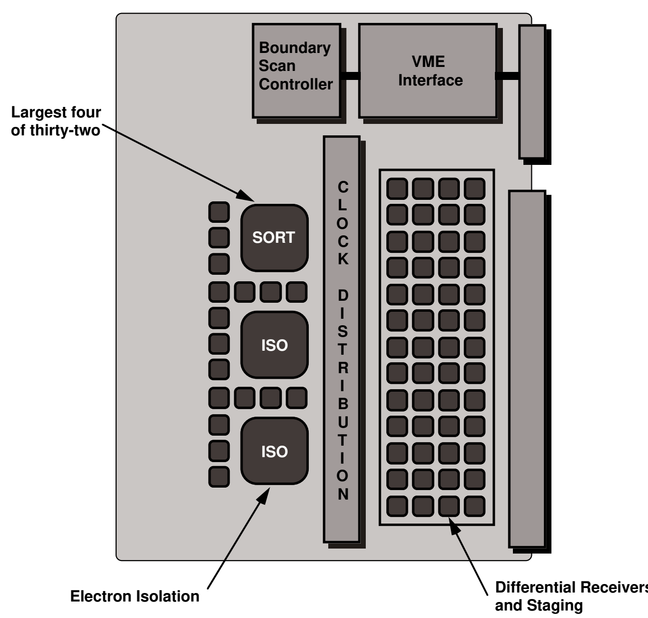

Figure 6. The Electron Isolation Card.

The Electron isolation algorithm will be implemented in a custom ASIC. The results from this Isolation ASIC are sorted in a second ASIC (Sort ASIC) and the top four candidates from the 4 x 8 trigger tower region are transferred to the Jet Summary card.

The Isolation ASIC is designed to shift in the data for 16 towers, 4 towers at a time, over a single bunch crossing time. The data for the 20 neighboring towers is also be loaded in the same time period. The entire 4 x 8 region is processed by two ASICs in four 160 MHz cycles.

The output of the ASIC is four 2-tower sums, with eight bits of dynamic range, and four 1-bit results indicating whether the eight nearest neighbor hadronic sums are $\leq$ 2.0 GeV. These results are produced every 6.25 nsec. In parallel with the Isolation ASIC are a set of lookup tables which use the same input information to determine H/E for each of the reference towers. The four 2-tower sums from the Isolation ASIC are combined with the two single bit results from the hadronic sum and H/E cuts and presented to a programmable look-up table which ranks the electron trigger results.

These ranks, one per reference tower, are presented in parallel to a single Sort ASIC. The Sort ASIC receives all 32 ranks from the two Isolation ASICs in one crossing and appends 5 bits of location information to each input. The 5-bit location follows each datum through the Sort ASIC and uniquely identifies the four largest. The resultant from the ASIC is the four highest ranks from the 4 x 8 trigger tower region.

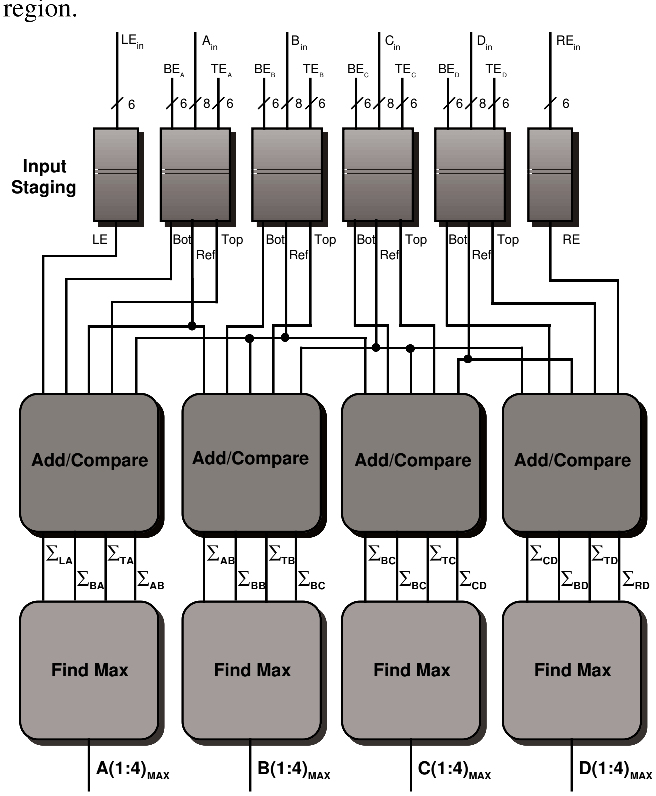

Figure 7. Block diagram of the Electron Isolation ASIC.

The Isolation ASIC, shown in Figure 7, handles four electromagnetic energies on an 8 bit scale, every 6.25 nsec. Nearest neighbors are also included in the data flow. During the first cycle of every crossing the four neighboring energies from the adjacent 4 x 4 region (top) are strobed into the ASIC. The neighbors along either edge of the 4 x 4 region, are also included, two at a time (left and right edges), during each 6.25 nsec period. Finally, the last cycle strobes in the four neighboring towers of the bottom edge. The nearest neighbor corners are not required by the algorithm. Thus, in one bunch crossing time, a total of 36 towers are clocked into the Isolation ASIC. All the neighboring electromagnetic energies are provided as the top 6 bits of the 8 bit range used for the reference towers.

The Isolation ASIC also handles the hadronic tower data necessary to check for hadronic isolation around individual towers. All neighboring hadronic information is on a 2 bit scale. The only outputs are the four electromagnetic and four hadronic results. Four two tower sums, on an 8 bit scale, and four corresponding 1 bit hadronic isolation flags are produced each 6.25 nsec.

Lookup tables are used for two separate functions. The first is to calculate the H/E cut. This operation is performed in parallel with the processing in the Isolation ASIC. Eight memories, cycling at 160 MHz, receive four bits of the hadronic information combined with four bits of electromagnetic information, producing an 8-bit address into the H/E lookup table. A single output bit is used to indicate, when true, that H/E < 0.05. The full 4 x 8 trigger tower region is processed in one crossing, which is slightly less than the time required by the Isolation ASIC.

A second set of lookup tables are used to produce a ranking of the electron trigger information based on the 8-bit sums, hadronic isolation from the Isolation ASIC, and the single bit result from the H/E cut. These 10 bits are used as an address into the lookup tables and will produce a value of 6 bits in length which represents a ranking of the different trigger categories resulting from the data. The memories will be cycled at 160 MHz. Therefore, one bunch crossing is required to produce the ranking information for the 4 x 8 region.

In order to limit the amount of information transmitted from each Electron Isolation card and each regional trigger crate, we have chosen to send only the four highest ranked trigger categories from each Electron Isolation card to the Jet Summary card. These four values have not been put in any particular order. Jet Summary card receives a total of 32 values from 8 Electron Isolation cards and sorts these again to determine the four largest values. The E_T information sent to the Jet Summary card from the Receiver card is also sorted to determine the four 4 x 4 subregions with the largest energy deposition.

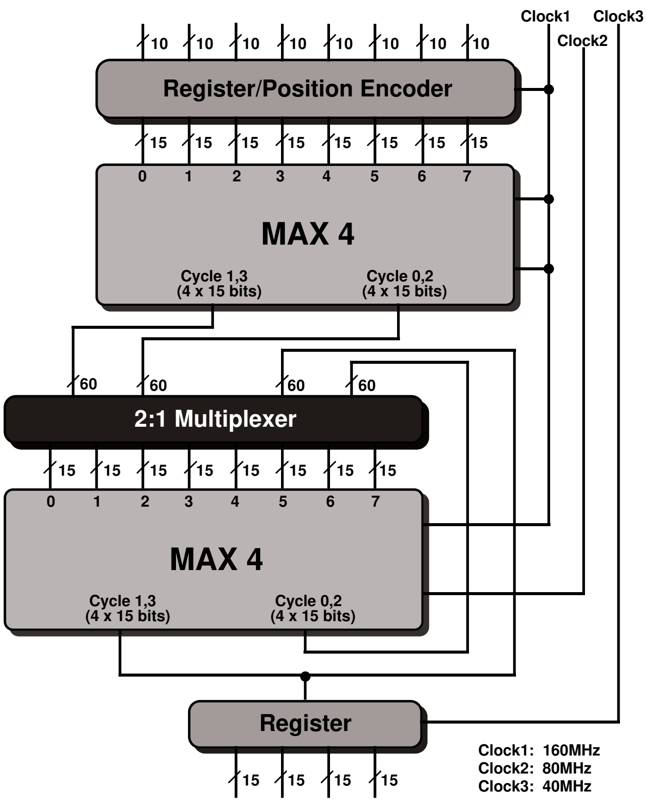

Figure 8. Sort ASIC block diagram.

The Sort ASIC is designed to find the four largest of thirty-two 10-bit values. Ten bits is sufficient to handle both the E_T sums and the trigger category information. Figure 8 is an illustration of the major functional blocks that make up the ASIC. The data is shifted in, eight operands at a time, over four 6.25 nsec cycles.

The algorithm implemented within the Sort ASIC is based on a simple rotation of operands. The eight operands are divided into two groups of four. The operands are compared in pairs between the two groups, with the larger of the two taking over the position of the left hand member of the pair. This comparison is performed in four stages with a rotation of compared pairs occurring between each stage. By the end of the fourth stage a sufficient number of comparisons have been made to ensure the four largest values are in the left-hand group. In order to save steps, and thus minimize the total latency, these four values are not placed in any rank order. The final four values, produced by the global trigger processor, are ordered during the final sort.

5. JET SUMMARY CARD

The Jet Summary card is shown in figure 9. It sits near the middle of the trigger data processing section of each regional trigger processing crate, as shown in figure 3, situated in the front portion of the crate between the 4th and 5th Electron Isolation cards. It collects and summarizes data from both the Receiver cards and the Electron Isolation cards at 160 MHz. The Jet Summary card has the same form factor as the Electron Isolation card, 9U x 280mm

The electron trigger rank information from eight Electron Isolation cards (32 values) is sorted to produce the four highest ranked electron triggers. These values have a 4-bit address appended to them which indicates which 4 x 4 trigger tower region, covered by the crate, produced them. The E_T values from the Receiver cards are also produced with a 4 x 4 tower granularity. These values are summed by a pair of Adder ASICs to produce a total E_T sum. The same information is processed by a Sort ASIC to determine the four largest 4 x 4 tower E_T values produced by the crate. This is used as the jet trigger. The E_T information from the Receiver card is also sent to memory lookup tables which generate E_X and E_Y for each 4 x 4 region. The E_X and E_Y values are summed individually in the Adder ASICs to produce total E_X and E_Y for the 256 tower region of the calorimeter covered by the crate.

The Jet Summary card also contains space for logic to search for tau candidates and perform luminosity monitor sums.

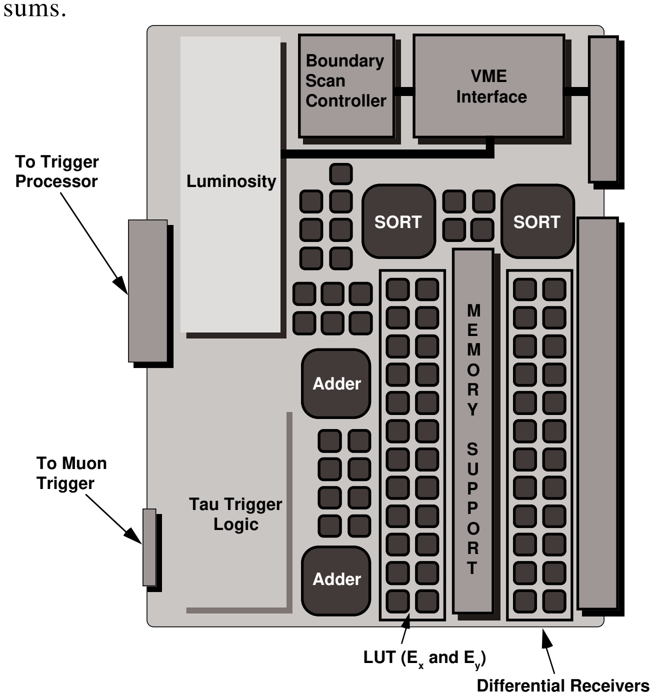

Figure 9. Jet Summary card.

The jet summary card transmits from each crate to the global calorimeter trigger 12 bits each of E_T, E_X and E_Y , 40 bits for the top 4 Jets, 24 bits of electron trigger rank, 4 bits of Jet E_T threshold information, 16 bits of location for the top 4 electrons, and 16 bits of information for the top 4 jets.

This work is supported by the United States Department of Energy and the University of Wisconsin.