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A Flash Analog-to-Digital Converter for Trigger Tests with the ATLAS Calorimetry

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Abstract

A system of FADC modules was developed as part of the RD27 project. Each FADC board is a standard 6U VME slave module, containing 4 channels of Analog-to-Digital Conversion with 8 bit resolution. An external clock input allows sampling rates of more than 80 MHz. The key feature is the front-panel output of digitized data in real time to a subsequent trigger logic.

In addition each FADC channel is equipped with a scrolling memory of 256 byte. The last 256 FADC samples can be read out, when digitization is stopped by a Gate signal. The memory is also 'write' accessible from VME. This permits writing of real test-beam data back to the memories. A special operating mode allows 'playback' of those data to the front-panel connector for tests of trigger logic in the laboratory.

0. Introduction

The aim of the RD27 collaboration is the design and test of key components for Level 1 trigger systems, to be built for the LHC experiments. One example is the design of the ATLAS Level 1 trigger, which requires digital input from calorimeters. The basic trigger granularity in ATLAS are cells of size $(\Delta\eta*\Delta\phi)=(0.1*0.1)$. Such cells are formed by summing up signals from corresponding calorimeter read-out channels **[Ref.1]**.

The Test- and Demonstrator- program, to be carried out at CERN-SPS beams, is based on 'small' detector prototypes, e.g. the LAr 'Accordion' calorimeter test module. Energy deposits in trigger cells are derived by analog summing. For tests of the Level 1 trigger, an interface is needed, which provides 8-bit digital values at the LHC bunch crossing rate of 40 MHz.

The FADC system, described below, was designed and built to fulfill this basic and a number of additional requirements. It is based on a system, which was successfully operated in joint RD27/RD33 tests (Level 1 Cluster Finder / 'TGT' LAr calorimeter **[Ref.2]**). The main components are the FADC boards, each containing 4 channels of Analog-to-Digital Conversion. The actual system consists of at least nine FADC modules (36 channels) housed in a CERN specified VME crate. This crate has an additional JAUX connector on the backplane, through which high power -5.2 Volt are supplied for ECL applications.

One auxiliary module provides level conversion (NIM-to-ECL) and a 1-to-16 fanout of this ECL-signal. The building block is implemented twice on the module, thus providing separate conversion and fanout for the 'Clock' signal as well as for the 'Digitization Gate' signal.

1. Description of the FADC module

1.1 Input/Output via the front-panel

The FADC board is a standard VME Slave-module of 6U height (double Euro-board). The layout of the front-panel is shown in **Fig. 1**.

There are four LEMO-type sockets (**IN 0-3**) to receive analog input signals. These inputs are terminated into 50 Ohm to match the impedance of the coaxial cable.

The FADC module requires a permanently running clock for the 'sampling' or 'playback' type of operation. This input must be supplied as 'differential ECL' to the 'twisted pair' socket labelled **CLK** on the front-panel.

The second 'twisted pair' input, labelled **DG** ('Digitization Gate'), controls the 'real time operation' of the module. The FADC module samples analog input signals (or 'plays back' data from memory) as long as an 'active' level is present.

These control signals are usually distributed from the auxiliary FANOUT module (see **Appendix A**).

The front-panel contains a set of four Light-Emitting-Diodes (**LED**s) for visual inspection:

* A LED called **CLK** shows the presence of a continous clock signal. The 'rising edge' of the clock is stretched to 100 ms. Thus, at clock frequencies > 10 Hz, the LED is permanently switched on.
* A LED labelled **PWR** shows the availability of all required supply voltages (+5V .AND. -5.2V) on board.
* A LED called **DG** indicates, that the 'Digitization Gate' is on. The module is either 'recording' or 'playing back'. In either case, digital data appear on the 64-pin connector with the frequency of the supplied clock.
* A LED labelled **VME** indicates any access from a computer over the VME bus.

The big **64-pin** IDC-type (e.g. 3M with clamps) connector provides real time output of the digitization result. The connector has its pin#1 on the bottom-right (label **21;** check triangle marker). The data are presented on the connector in the same vertical order as the analog channels enter the module (see **Appendix B** for a detailed description).

The following table shows the pin-layout of the connector in abbreviated form:

<u>ECL-levels for **Data-bit=1** (active):</u>

		-0.8 V (**+**label)	-1.6 V (**-**label)
IN 0:	MSB (bit 7)	63	64
	LSB (bit 0)	49	50
IN 1:	MSB (bit 7)	47	48
	LSB (bit 0)	33	34
IN 2:	MSB (bit 7)	31	32
	LSB (bit 0)	17	18
IN 3:	MSB (bit 7)	15	16
	LSB (bit 0)	1	2

1.2 The building blocks of one FADC channel

A block diagram of the FADC board is shown in **Fig. 2 [Ref.3].**

1.2.1 The analog line-receiver

Each analog input signal passes a line-receiver amplifier. A group of two channels with the corresponding LEMO sockets is implemented on a 'daughter' board. If need arises, a new board can be developed to accomodate other types of line-receivers, e.g. a differential receiver for balanced signals on 'twisted pairs' and/or amplifiers with non-linear gain characteristics.

The feed-back resistors, which determine the amplifier gain, are the only non-SMD devices on the present 'daughter' board. Wire resistors are easier to exchange in a test beam environment. The presently installed resistor value yields a gain of 2. This corresponds to an acceptance window of 0 to -1.25 Volt into the 8-bit FADC giving a LSB of 5 mV.

The input signal crosses AC-coupling capacitors to suppress DC and 'low frequency' contributions. However, a real LAr-signal [Ref.4] is not distorted.

1.2.2 The FADC

The FADC itself is an AD9012 with 100 MHz sampling capability. Its operation is driven by a strobe signal derived from the clock, which originates from the front-panel input.

Analog signals from the LAR 'Accordion' prototype are shaped in a 'bipolar' manner. There is a large negative amplitude (FWHM is ca. 2 LHC bunch crossings) and a small, but stretched, positive amplitude (FWHM is ca. 16 LHC bunch crossings). The amplitude ratio of negative/positive part of the signal is about 90% / 10% **[Ref.4].**

The FADC system must digitize both parts of the bipolar signal. This is achieved by implementation of a 'level-shifting' Digital-to-Analog Converter (DAC). The range of this device is also 8 bit (but 10 mV/step fixed), i.e. the resolution is identical to the FADC. Therefore, the 'zero-level' can be set to any value within the FADC range. The DAC is 'write' accessible from the VME bus. Its output level is fed to all four channels of one FADC board simultanously.

After the line-receiver, the analog input signal of each channel passes another amplifier (gain=1), where it is inverted and biased with the offset value coming from the DAC. Only then it reaches the FADC proper for digitization.

Tests in the laboratory have shown, that the whole FADC board can be safely operated at a clock rate of 80 MHz. This allows sampling of any analog input signal at twice the rate of LHC bunch crossings. Studies of subsequent components of the trigger system may benefit from this feature.

1.2.3 The scrolling memory

The FADC produces a byte of data at every clock cycle. The data are automatically transferred into a fast memory of size 8 bit * 256 locations. This covers a latency range of 6.4 µsec, when the clock rate is 40 MHz (normal LHC bunch crossing rate). The time range shrinks to 3.2 µsec at 80 MHz, but is still large enough to cover the foreseen length of the ATLAS level 1 pipeline (2.5 µsec).

The necessary addresses are generated by a revolving counter (0->255->0-> etc.), which is also stepped by the clock signal. Thus, the memory is continuously written/overwritten from the moment when the 'Digitization Gate' is set 'ON'. The memory content remains untouched when the 'Digitizaton Gate' goes 'OFF'. The state of the address counter (address of last FADC sample) is 'read' accessible from VME. Starting VME readout of the memory from this address backwards, the 'sampling history' over the entire latency range can be accessed from a Data-AQuisition (DAQ) computer.

The second equally important role of the memory is the 'offline playback' of acquired FADC data. The address counter as well as the memory are 'write' accessible from VME. Therefore, data can be loaded from the VME bus into the memory up to its capacity of 256 data bytes. The FADC module can then be set to 'playback' mode via VME. In this case, the external clock determines the 'playback' frequency of data to the front-panel connector. Start of 'playback' is given by the 'Digitization Gate' similar to the recording mode described above. Data from the memory are output in the same revolving manner as storing is done in recording mode. The 'Digitization Gate' going 'OFF' stops the 'playback'.

1.2.4 The real-time ECL output

The absolutly essential feature of the described FADC is the output of the data in real time for use in a subsequent trigger system. For this purpose the FADC data are converted to differential ECL signals, which are sent to the front-panel port.

<u>Technical Note:</u> It is mandatory to connect the VME-ground of the FADC crate to the signal ground of the following trigger crate with a large cross-section cable. The 64-pin ECL cable has no leads left to connect the two ground potentials for return currents.

1.3 The interface to VME bus

The FADC module is a standard slave with regards to VME specifications. Its address space spans 256 bytes starting from a base address. The full module address consists of 24 bits (A0-A23).

The top byte (A23->A16) is coded in a GAL (Generic Array Logic) to be currently 'C1' (changable by reprogramming the GAL).

The middle byte (A15->A8) identifies the individual FADC module. The lower five bits of this byte can be set by on-board jumpers. Thus, **32 modules can be addressed in total, i.e. 'C1 00 xx' to 'C1 1F xx'**.

Technical Note: jumper=IN is bit=OFF, jumper=OUT is bit=ON; LSB is near top-edge, MSB is near bottom-edge of board.

The low byte (A7->A0) contains function codes needed when accessing the FADC module from the VME bus (see chapter 2).
There are in addition two address modifiers (AM codes), which are recognized by the module. These are :

AM = '3B' -> 'Standard nonprivileged block transfer' D32,(A24).
AM = '39' -> 'Standard nonprivileged data access' (A24).

2. VME: Programming Model and Operating Modes

The functional access to the FADC module is limited to the lowest order byte (A7->A0) of the 24-bit address (e.g. C1_00_xx).

The following codes are defined within the low byte of the FADC module address (xx = value : VME_access_mode):

xx = 00: longword D32
Read/Write the byte-wide memories of chan#0 to chan#3: VME access is set to 'longword' mode (low->high byte = ch#0->3).

Technical Note: The address counter is incremented automatically in 'block transfer' mode.

----
xx = 00: word D16
Read/Write the byte-wide memories of chan#0 and chan#1: VME access is set to 'word' mode (low->high byte = ch#0->1).
xx = 02: word D16
Read/Write the byte-wide memories of chan#2 and chan#3: VME access is set to 'word' mode (low->high byte = ch#2->3).
----

xx = 04: word / longword D16/D32
Read/Write the memory address counter: The state of the counter being read arrives in the low byte (i.e. D0-D7). The value, setting the counter, has to be in the second byte (i.e. D8-D15).

xx = 06: word / longword D16/D32
Write only a value to the DAC: The relevant data, to set the 8-bit DAC (10mV/step), are contained in the low byte (i.e. D0-D7).

Technical Note: Due to the signal inversion (see 1.2.2) the DAC must be loaded with a 2-complement value, i.e. DAC = 255 - OFFSET (10mV/step).

xx = 80: word / longword D16/D32
Write and Read the Control/Status register. Both buffers are accessed on the same address.

The bit-allocation of Control/Status is displayed in **Fig.3.** Control- and Status-bits are interconnected by some logic, which should ensure that only 'legal' combinations of control-bits are set. 'Legal' combinations are settings, that lead to proper operating modes of the FADC module.

Technical Note: Selective Bit-Setting is not possible. Always the full byte must be supplied for 'write' containing the changed bit.

The meaning of the individual data bits is for:

'Write'

D0 unused

D1 unused

D2 Source of 'Digitization Gate'
=0 :internal from program via VME
=1 :external from front-panel
NOTE: An external Gate signal is privileged,
i.e. a clock and an external gate set the FADC
always in BUSY mode.

D3 Run mode
=0 :Sample an analog input on front-panel
=1 :Play back data from memory loaded via VME

D4 Level of 'Digitization Gate' from program
=0 :set DG = OFF from program
=1 :set DG = ON from program

D5 unused

D6 Reset programming error
=0->1->0: write a 'pulse' to reset the flip-flop

D7 Reset clock error
=0->1->0: write a 'pulse' to reset the flip-flop

'Read'

D0 Clock status
=0 :clock missing
=1 :clock detected (> 10Hz)

D1 Status of external 'Digitization Gate' (front-panel)
=0 :DG = OFF
=1 :DG = ON

D2 Busy status of FADC module
=0 :FADC module idle
-> VME access to memory data allowed
=1 :FADC module busy:
-> recording or playing back; VME access only to control/status register allowed

D3 Run mode status
=0 :Digitizing (recording) analog input on front-panel
=1 :Playing back data from memory loaded via VME

D4 Internal 'Digitization Gate' status
=0 :Internal DG = OFF
=1 :Internal DG = ON

D5 unused

D6 Programming error status
=0 :OFF
=1 :Prog. error stored in flip-flop

D7 Clock error status
=0 :OFF
=1 :Clock error stored in flip-flop

Technical Note: The flip-flops are not automatically reset, when the error disappears. The 'reset' must be done explicitly from the program.

The FADC module can be readout in normal VME 'single word' mode or 'block transfer' mode, where the address counter provides the stepping through the memory space.

Furthermore, Direct Memory Accces (DMA) can be performed with a VME master, which can handle this most efficient mode for bulk data movement.

3. Test Procedures and Performance Results

The set-up for tests in the laboratory consists of the following components:

* An 'Arbitray Funtion Generator' (LCR-AFG9109), which produces the analog input to one FADC channel. A parametrized 'real' pulse from the LAR 'Accordion' prototype with a periodicity of 2 μsec (see chapter 3.1).

* A VME crate with a master CPU (CES-FIC8234) for VME control and and a second VME crate, connected over a VIC tree, for readout of the FADC slaves.

* A Logic Analyser (TEK-3001GPX) to check the data output on the front-panel connector.

3.1 Laboratory Tests for production control

Each channel of every FADC module was checked in the following manner:

* The FADC was driven permanently by an external clock (40 or 80 MHz NIM signal from a pulse generator, which was converted to ECL in the auxiliary FANOUT).

* Analog input from the AFG was fed to the indiviual channel.

* The FADC operation was controlled by a stand-alone program **[Ref.5]** running on the FIC-CPU. Offset values through the DAC can be applied from the program and the 'Digitization Gate' can be switched 'ON/OFF'. The sampling history, stored in the memory, is read out and displayed as histogram on a data terminal. The program can check all operating modes of the FADC as well as the different VME features, like word or longword access and DMA readout operation over a VIC tree.

* Test of the 'real time' output at the front-panel had to be performed with a Logic Analyser. The differential ECL signals were recorded synchronously to the FADC clock and stored.

Linearity of the FADC and compensation of output offsets from analog components were checked using the on-board DAC.

Checking the correctness of the FADC data was done by comparing quantitativly pulse-shape and -amplitude of the periodic signal
a) on the DOS-PC controlling the AFG (input).
b) the memory histogram (online output on VME bus)
c) the Logic Analyser histogram (real time output).

4. Installation in Test Beam H8 at CERN-SPS: Tests with DAQ system and BCID module

A complete VME crate with nine FADC modules and one Level-converter/Fanout was installed in May 1995 at the CERN-SPS (H8). First checks with a sine-wave input and the software, developed on the DAQ-system in the testbeam, showed that the FADC system is functioning correctly.

Finally, after cabling up the front-panel output to the BCID (Bunch Crossing IDentificaton) module, comparisons of the FADC memory content and the content of the front-end memories on the BCID module showed identical results. This certifies, that the FADC data can be successfully used in real time for trigger applications.

5. Conclusion

We have designed and built a Flash-ADC system of more than 36 channels for the ATLAS tests. It digitizes calorimeter signals in real time for the ATLAS prototype of a trigger level 1 processor. The operation in a testbeam has already shown satisfactory results. This FADC system is based on standard, commercially available components, which are used on standard VME modules.

It is envisaged to extent this system for tests with other parts of the ATLAS calorimetry (el.-mag. and hadronic endcaps, hadronic 'tile' calorimeter and combinations of those). The number of channels needed to test trigger performance is not completely defined. Similarly, signal characteristics from the other detectors must be studied. Flexibility, to adapt to different requirements, is foreseen (e.g. line-receiver on 'daughter' boards). There is common understanding, that this system shall be used for these tests with minor modifications.

The experience gained in the building of this 'real time' FADC system is of great value for further design efforts towards a final trigger front-end system for ATLAS. It is clear, however, that integration (usage of ASICs) has to be pushed much further to arrive at a system, which copes with the number of trigger channels in ATLAS proper.

Contents:

Figures:

Appendices:

References:

[1] The Demonstrator Program for the ATLAS Level 1 Trigger, Backup Document to the ATLAS Technical Proposal, RD27 Note #35 or ATLAS Note# DAQ-NO-31, January 1995

[2] The Calorimeter Trigger, C. Geweniger et al. TGT-Note 94-049

[3] Schematics of the FADC board, J. Krause, IHEP Heidelberg, November 1994

[4] Study of pile-up in the ATLAS e.-m. Calorimeter, ATLAS internal note CAL-NO-73, February 1995

[5] FADC Test Program, C-source available on request from B. Rensch, IHEP Heidelberg, January 1995

FADC for ATLAS-tests (Front-Panel)

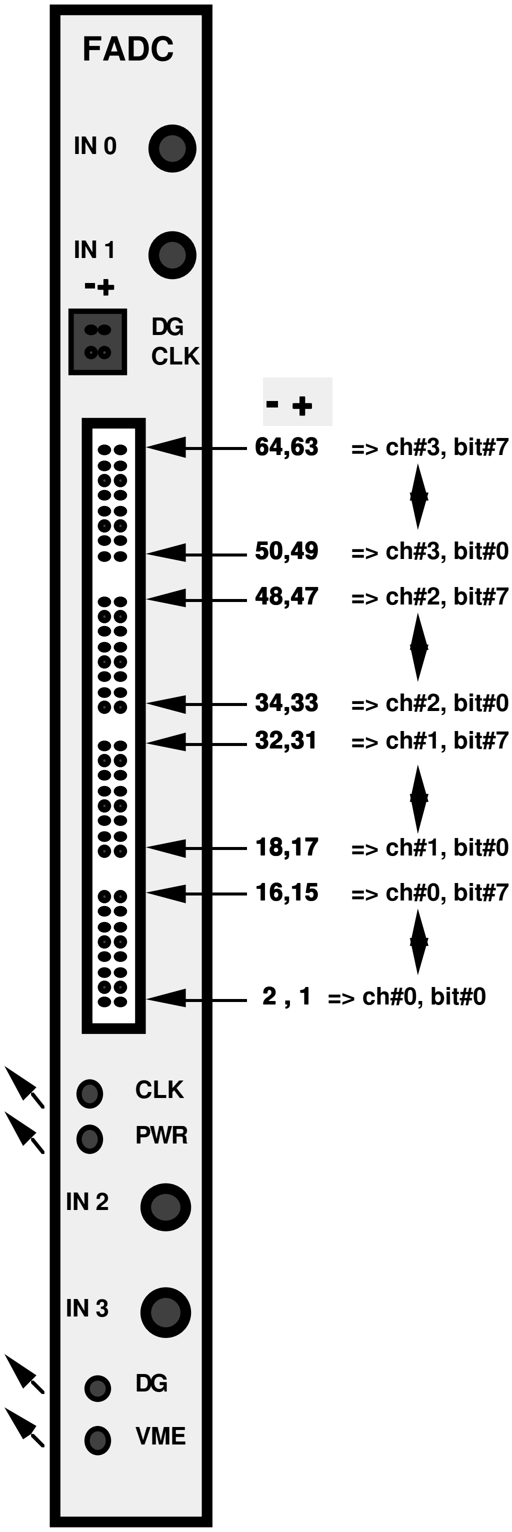


Figure 1

FADC for ATLAS-tests

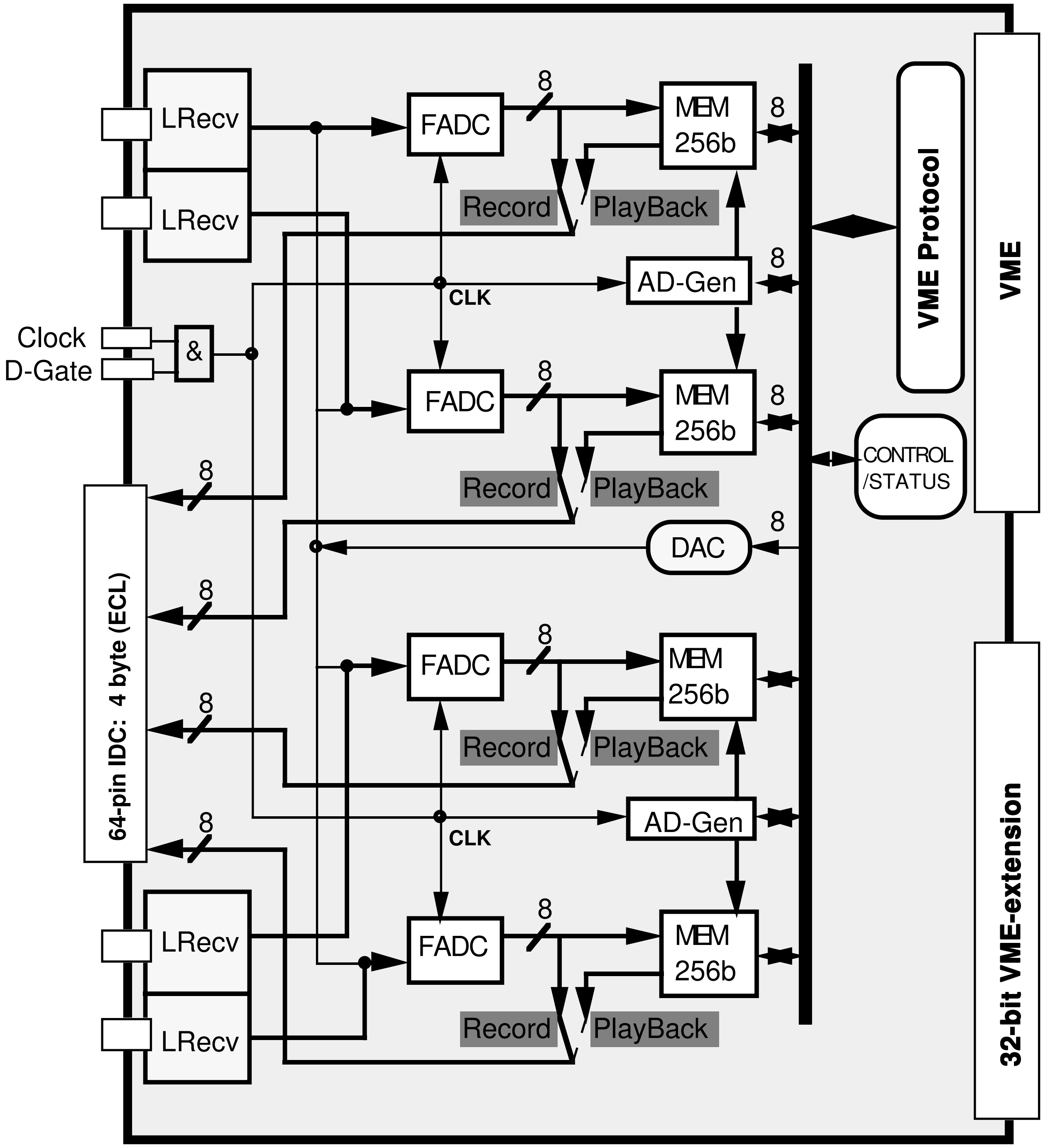


Figure 2

FADC for ATLAS-tests (Control/Status)

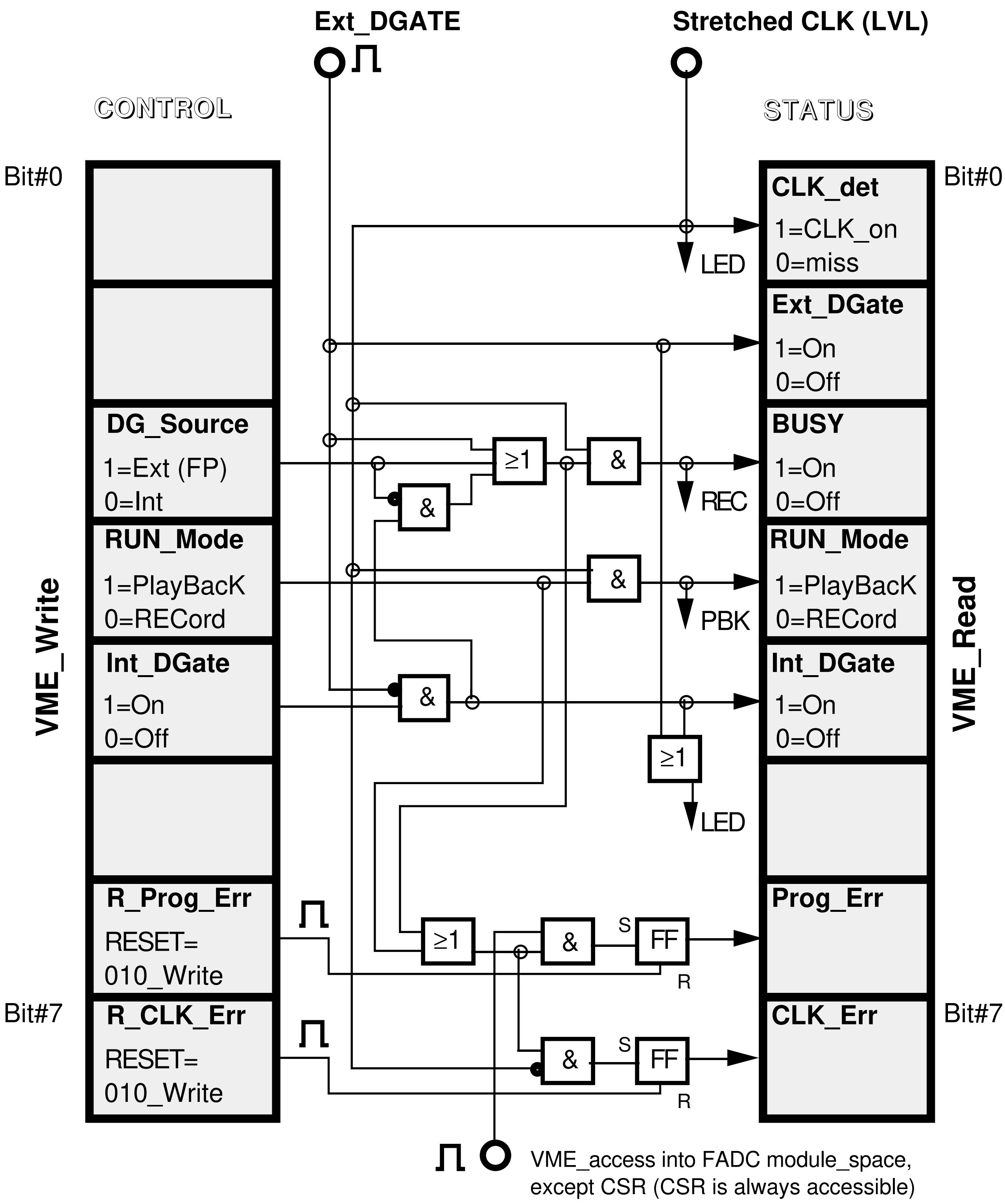
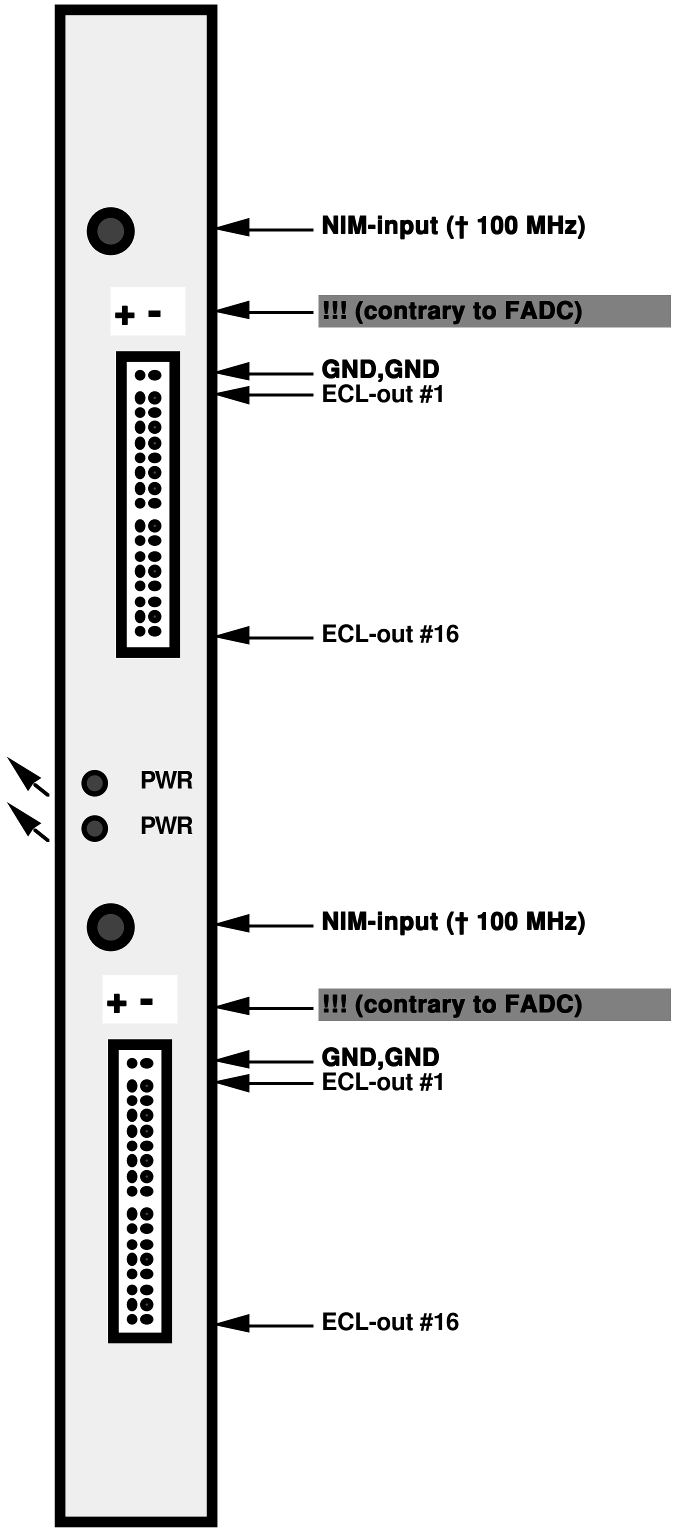


Figure 3

Two-fold NIM->ECL Converter/Fanout (Front-Panel)



Appendix A

REVISED HEIDELBERG FADC CONNECTOR PIN ALLOCATION

CONNECTOR IS 64 WAYS IDC.

		"+" Quiescent = low ie logic 0. Active = high ie logic 1. PIN No.	"-" Quiescent = high ie logic 1. Active = low ie logic 0. PIN No.
Channel 3	Bit 0	1	2
	Bit 1	3	4
	Bit 2	5	6
	Bit 3	7	8
	Bit 4	9	10
	Bit 5	11	12
	Bit 6	13	14
	Bit 7	15	16
Channel 2	Bit 0	17	18
	Bit 1	19	20
	Bit 2	21	22
	Bit 3	23	24
	Bit 4	25	26
	Bit 5	27	28
	Bit 6	29	30
	Bit 7	31	32
Channel 1	Bit 0	33	34
	Bit 1	35	36
	Bit 2	37	38
	Bit 3	39	40
	Bit 4	41	42
	Bit 5	43	44
	Bit 6	45	46
	Bit 7	47	48
Channel 0	Bit 0	49	50
	Bit 1	51	52
	Bit 2	53	54
	Bit 3	55	56
	Bit 4	57	58
	Bit 5	59	60
	Bit 6	61	62
	Bit 7	63	64

Appendix B ***3rd October 1994***