CMS CALORIMETER LEVEL 1 TRIGGER CONCEPTUAL DESIGN

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1. Introduction

1.1 CMS Trigger and Data Acquisition System

The CMS trigger and data acquisition system [1] is designed to operate at the nominal LHC design luminosity of 10^{34}, where an average of 20 inelastic events occur at the beam crossing frequency of 25 nsec. This input rate of 10^9 interactions every second must be reduced by a factor of at least 10^7 to 100 Hz, the maximum rate that can be archived by the on-line computer farm. CMS has chosen to reduce this rate in two steps. The first level stores all data for approximately 3 microseconds, after which no more than a 100 kHz rate of the stored events is forwarded to the second level. This must be done for all channels without dead time. The second level is provided by a subset of the on-line processor farm, and passes a fraction of these events for more complete processing by the remainder of the on-line farm. During the 3 microseconds of the level 1 trigger processing time, trigger decisions must be developed that discard a large fraction of the data while retaining the small portion coming from interactions of interest.

1.2 Level 1 Calorimeter Trigger System Function

The CMS level 1 trigger decision is based in part upon local information from the level 1 calorimeter trigger about the presence of objects such as photons, electrons, and jets, as well as global sums of E_t and missing E_t (to find neutrinos). Each of the objects, such as electrons, muons and jets, are required to pass a series of p_t or E_t thresholds, which are used in making the Level 1 Trigger Decision.

1.3 Electron/Photon Trigger

The electron/photon trigger is based on the recognition of a large and isolated energy deposit in the electromagnetic calorimeter. The isolation requirements ask for a small amount of energy deposited in the calorimeter trigger towers surrounding the ECAL energy cluster, as well as a small hadronic energy deposited in the HCAL in the cluster region. There are different thresholds for inclusive electrons/photons, dileptons, and for very high E_t electrons. The isolation cuts are relaxed and finally eliminated for

triggers with increasing E_t thresholds. The tightest set of cuts is used only to push the electron and photon thresholds to the lowest possible E_t values.

The algorithm implemented in the hardware design involves two separate cuts on the longitudinal and transverse isolation of the ECAL energy deposit. The first cut involves the hit tower HCAL to ECAL energy ratio, H/E < 0.05. A second cut requires transverse isolation, i.e. a cut on a sum of HCAL transverse energies in the nearest eight towers surrounding the hit tower, H1 < 2.0 GeV. In order to reduce the number of bits of information exchanged between electronics cards we limit the dynamic range of neighboring tower HCAL information to 2-bits. Overflows of both the 8-bit scale for ECAL and central HCAL towers, and the 2-bit scale for neighboring HCAL towers are treated as maxima. The electron/photon trigger algorithm is illustrated in Figure 1.

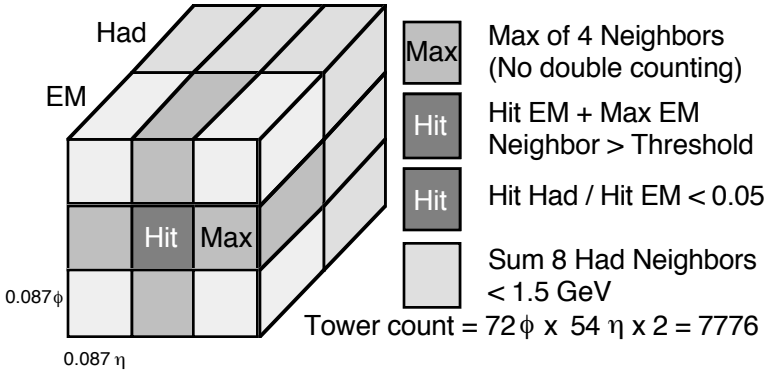

Figure 1. Level 1 Electron Trigger Algorithm.

1.4 Jet and Isolated Hadron Triggers

The jet triggers are based on sums of 0.35 x 0.35 eta-phi regions using a dynamic range that covers energies up to about 250 GeV. A second category of jets that exhibit the presence of isolated hadrons can be found by testing the high E_t 0.35 x 0.35 regions to determine if a high fraction of the total observed energy is contained in a single trigger tower. Such regions are candidates for isolated hadrons. These isolated hadron jet triggers are used in detecting tau's. Jet triggers will be used in combination with electron/photon, muon and other jet triggers. For these combinations of triggers, lower E_t jet thresholds will be employed.

1.5 Missing E_t and Sum E_t Triggers

Neutrino identification consists of calculating the event missing E_t vector and testing it against a threshold. The calorimeter trigger calculates both sums of E_t and missing E_t. The transverse energy vector components are calculated from the 8-bit compressed-scale digitized HCAL and ECAL pulse

heights converted to a linear scale with a 10-bit dynamic range, and multiplied by entries in lookup tables containing the tower angular coordinates. The HCAL and ECAL sums are then combined into single tower sums. The tower sums over threshold are routed through the digital summing networks. The E_t trigger is not used as a standalone trigger, but only in combination with other triggers. When pre-scaled by factors of 1000 or more for E_t above 100 GeV, it is also used to check trigger efficiency and measure the E_t spectrum.

1.6 Luminosity

Operating the LHC requires continual non-intrusive measurement of relative luminosity and periodic intrusive measurement of the absolute luminosity using an absolute measurement. The non-intrusive measurement of relative luminosity can be done with signals accumulated in the level 1 calorimeter trigger system. The level 1 calorimeter trigger system provides four thresholds on the energy in each 0.7 delta-eta x 0.7 delta-phi calorimeter tower. The lowest threshold is set to have a rate 100 kHz. The granularity is set by the need to have a significant rate and the ability to observe localized "hot spots" in the calorimeter. The thresholds are determined by the nominal precision of 1% every 1/10 second, implying a count rate of 100 kHz. In order to fulfill this requirement, the following data requirements are set:

Provided every 0.1 sec:

> Total number of 0.7 x 0.7 towers with energies above each of 4 individually programmable thresholds. This consists of 4 16-bit numbers.
>
> Time interval in crossings over which the number of towers above were accumulated.

Provided every 5 minutes:

> Number of times each of 2,835 crossings has a 0.7 x 0.7 tower over a threshold, independently programmable from the four listed above. If a particular crossing has N 0.7 x 0.7 towers that exceed this threshold in a single accelerator cycle, then the sum for this crossing is incremented by N. This enables the luminosity per crossing to be accumulated for analysis of occupancy and deadtime effects.
>
> Number of times each 0.7 x 0.7 tower region exceeded the single threshold listed above.
>
> Time interval in complete accelerator cycles over which the number above was accumulated.

This information is provided over the DAQ data transmission network from the DAQ processors in the level 1 calorimeter trigger crates. The rate of transmission of this data will impose a negligible burden on the DAQ system.

1.7 CMS Level 1 Trigger System

The CMS Level 1 Trigger system is a deadtimeless processor that operates on a subset of the full data collected from each LHC beam crossing every 25 nsec. The Level 1 Trigger System analyzes the subset of data within a fixed amount of time to determine if the data collected from the beam crossing is to be discarded or held for further processing by the higher level trigger systems.

The Level 1 Trigger System is comprised of the front end electronics that generate trigger primitives on the detector, and the Level 1 processing logic in the electronics barracks. The Level 1 logic and front end electronics are interconnected both electrically and optically to form multiple pipelined data streams, which come together at the Level 1 Global Logic to generate a Level 1 Accept/Reject for the detector.

1.8 Input Data to the Level 1 Calorimeter Trigger

The front end electronics will operate and sample the input calorimeter pulse height at 80 MHz and use this information to produce a trigger tower sums at 40 MHz. These trigger sums will emerge in 13 (25 nsec) crossings after the input pulse height reaches the front end electronics. The front end electronics for the baseline design is the fully digital FERMI readout system [2].

The calorimeter level 1 trigger system receives digital trigger sums via optical fibers from the front end electronics system, which transmits energy on an eight bit compressed scale. The data for two HCAL or ECAL trigger towers for the same crossing will be sent on a single fiber in eight bits apiece accompanied by five bits of error detection code. The compressed scale of the trigger tower data will be derived from memory lookup tables within the front end system. Programmable tables will enable full flexibility to modify the compression algorithm as required. The Trigger system will use memory lookup tables to decode the 8-bit compressed scale data into a linear scale with a 10 bit dynamic range in the adder tree.

There is a 1:1 correspondence between HCAL and ECAL trigger towers. The trigger tower size is equivalent to the HCAL physical towers, .0873 x .0873 in eta x phi. The phi size remains constant in delta-phi and the eta size remains constant in delta eta down to an eta of 2.1, beyond which the eta size doubles. There are 3888 total ECAL trigger towers and 3888 total HCAL trigger towers from eta = -2.6 to eta = 2.6 (54 x 72 eta-phi divisions).

The very forward calorimeter (VFCAL) region will sum electromagnetic and hadronic energy for one tower into a single trigger sum. The trigger towers

will be divided more coarsely in phi and eta, possibly in 18 phi bins by 4 eta bins from |eta| = 2.6 to 4.0 and then 9 phi bins by a single eta bin to |eta| = 5.0. Beyond |eta| = 3.0, where the HCAL ends, the front end calorimeter electronics will have a different interface to the different calorimeter technology for the VFCAL, but will still provide the same type of single tower outputs. Therefore we estimate at most 3888 ECAL, 3888 HCAL and 162 VFCAL trigger channels for a total of 7938 trigger channels carried on 4050 fibers.

1.9 Overview of Calorimeter Level 1 Trigger Design

This document outlines a conceptual design for the level 1 calorimeter trigger. A block diagram of the CMS Level 1 Calorimeter trigger system is shown in Figure 2. General considerations that have been emphasized in this conceptual design include access to components, power, space and cooling requirements, diagnostics, efficiency and performance information, backplane traffic and timing, DAQ and timing interface, and I/O connections. The design is implemented using off-the-shelf technology wherever feasible, e.g., 10KH and ECLiPS ECL, TTL, and CMOS components. ASICs are used only where fully justified. The logic design maximizes flexibility and programmability by using memory lookup tables.

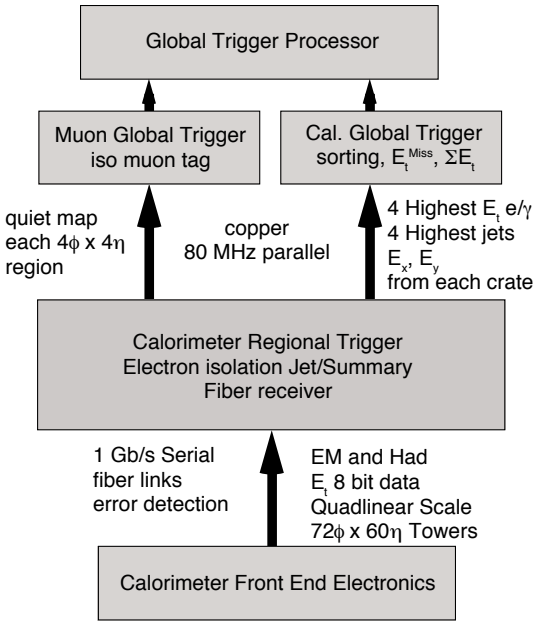

Figure 2. Level 1 Calorimeter Trigger Overview and details of one crate.

2. Calorimeter Regional Trigger Crates

There will be 19 calorimeter processor crates covering the full detector. Eighteen crates are dedicated to the barrel and two endcaps. These crates are filled out to an eta of 2.6, with partial utilization between 2.6 and 3.0. The remaining crate covers both Very Forward Calorimeters. Our intention at

present is to locate two crates each in Aleph-style racks. The remaining rack front panel space will be occupied by fans, heat exchangers, and crate power supplies. Front panels will be used at all card locations to provide an enclosed environment for the chilled air.

The crate, shown schematically in Figure 3, is based on standard Eurocard hardware. It is likely, however, that construction will require some custom fittings. The height is 9U and the depth approximately 700mm, as determined by the front and rear card insertion. The Aleph rack dimension (900mm deep) can handle the crate depth with some reserve for cabling, plumbing, and other services. The backplane is completely custom with a full 9U height. The top 3U is reserved for a 32 bit VME interface. The remaining 6U is used for the high speed data paths between individual cards. The front section of the crate is designed to accommodate 280mm deep cards, leaving the major portion of the volume for 400mm deep rear mounted cards.

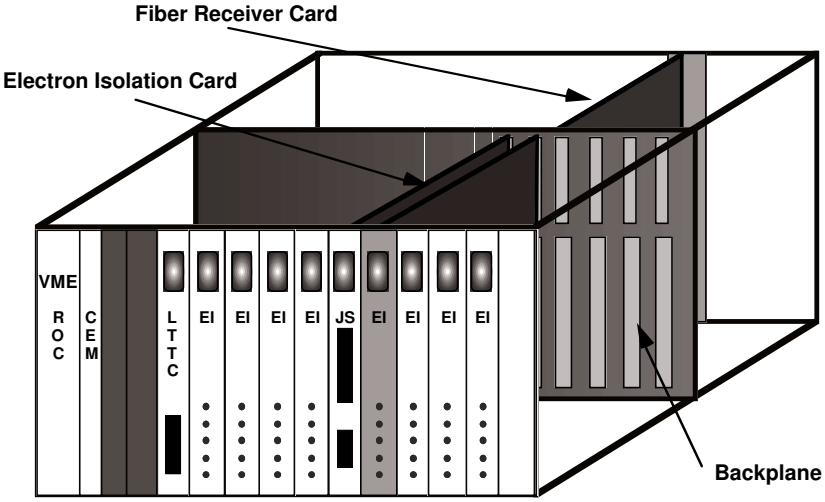

Figure 3. Schematic view of a typical Calorimeter Level 1 Regional crate.

Power supplies will be mounted in a separate chassis either above or below each crate. They will be located in the forward 280mm of the volume in consideration of the lower heat load (per unit area) of the forward cards. It might be desirable to put the supplies above the crates just to keep the cards closer to the heat exchangers. Testing is required to determine whether this up and down arrangement will be successful. On board DC - DC converters are also being considered as possible solution to power distribution.

2.1 Enumeration of Card Types

The majority of cards in the Calorimeter Level 1 Regional Processor Crates, encompassing three custom board designs, are dedicated to receiving and processing data from the calorimeter. There are eight rear mounted Receiver cards, eight front mounted Electron Isolation cards, and one front mounted Jet Summary card for a total of 17 cards per crate dedicated to processing data from the calorimeter.

In addition, there are several support cards. The first of these is a readout crate controller and communication module (ROC) provided by the DAQ group. The second is a crate environment monitor (CEM) which may or may not be a commercial board. The decision to purchase or create a custom design will depend on the final requirements of the environmental monitoring system. Finally, there will be a card dedicated entirely to clock distribution and logging status for the cards in the data processing path. This card, the Local Timing, Trigger and Control card (LTTC) will interface to the detector Timing, Trigger and Control (TTC) distribution system via the timing receiver ASIC produced by the TTC group [3].

2.2 Crate Backplane

As mentioned above, the backplane is a monolithic, custom, 9U high printed circuit board with front and back card connectors. The top 3U of the backplane holds 4 row (128 pin) DIN connectors, capable of full 32 bit VME. The first front slot of the backplane will, however, use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. Thus, a standard VME system module can be inserted in the first front station with a form factor conversion between the first slot and remaining slots performed on the custom backplane. The second front card position may also be designed with standard 96 pin DIN connectors if the crate monitor requires them. VME terminations will reside on the backplane.

The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high speed, controlled impedance, connector for both front and rear insertion at each card position. The design is based around a 340 pin connector, by AMP Inc, to handle the high volume of data transmitted from the Receiver cards to the Electron Isolation and Jet Summary Cards.

The AMP 340 pin connectors have a powerplane between every four signal pins, producing a stripline impedance of 50Ω. Separate high current contacts, provided for the powerplane connections, will be used to transmit power to the boards. The connectors are housed in a cast aluminum shell that doubles as a board stiffener. The electrical characteristics of the connectors are excellent, allowing rise times in the sub-nanosecond region with very low crosstalk. Press fit contacts are available for use on the backplane. The mating force required for the 340 pin AMP connector is approximately 190N. The four row DIN connector requires an additional 109N. For comparison, a standard 9U, three connector system requires a total of 244N. Therefore, the mating force is on the order of what is encountered in a standard 9U Eurocard system.

2.2.1 Number of Slots

The front and rear insertion of cards in the data processing section of the crate was chosen to allow greater separation between cards and to provide a more protected environment for the fibers connected to the rear mounted Receiver

cards. The increased separation will promote better cooling of the cards, and will enable a wider selection of front panel components. The staggering of the slots between front and rear cards, shown in Figure 4, is as much a result of the style of connector selected as the fact that piggybacking of connectors is inappropriate in this situation. Almost half of the signals entering the Electron Isolation board come from neighboring Receiver cards.

The spacing between cards, in the data processing area, is 3.05cm front or rear, with a 1.52cm stagger front to rear. Therefore, the eight Receiver cards, eight Electron Isolation cards, Jet Summary card, and Clock distribution card occupy 18 slots with a span of only 27.43cm across the front of the crate. The remaining 13.21cm will be allocated to a DAQ Readout card (ROC) (4.06cm), Crate Environment Monitor (CEM) (2.03cm), and a transition region for the change in form factor between the standard and non-standard VME. This is a total of 20 slots. The unused space amounts to about 5.08cm after allowing for the transition region. This represents a dedicated contingency for future additions or changes to the design.

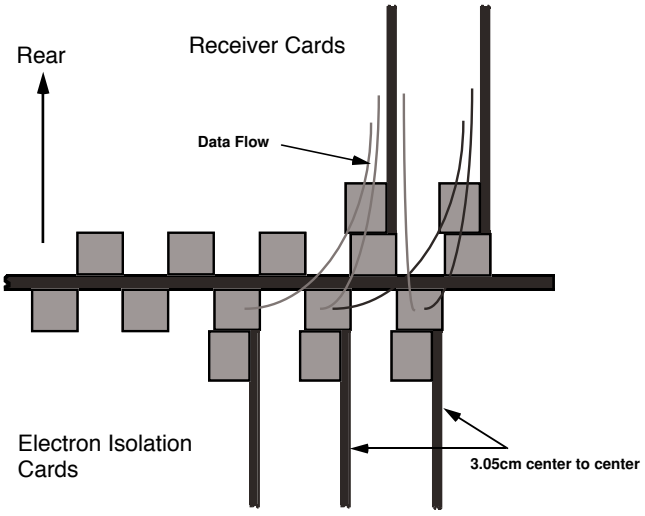

Figure 4. Top view of region crate backplane.

2.2.2 Card Order

As shown in Figure 3, the first two or three slots in the crate will house the Crate Readout Card (ROC) and Crate Environment Monitor (CEM). The remaining crate volume is used for the data processing cards. The first card after the transition region will be the Local Timing Trigger and Control card (LTTC). This is followed by the first four Electron Isolation cards (EI) with their corresponding Receiver cards (RC) staggered 1.52cm to the right in the rear of the crate. The next card is the Jet Summary card (JS), with no matching Receiver Card. Finally the four remaining Electron Isolation cards fill out the crate. The corresponding Receiver cards are plugged in at the rear, staggered 1.52cm to the left. The figure is not to scale in that it implies

substantially more free space at the right hand end of the crate than actually exists.

2.2.3 Backplane construction

The backplane will be a 41.91cm x 39.70cm multilayer printed circuit board, between .32cm and .36cm thick. The final thickness will depend upon the tradeoffs necessary to achieve the required impedance and proper mechanical strength with standard core stock and pre-preg. There will be on board VME terminations, multiple studs for power supply connections, bypass capacitors, and mounting holes.

The design impedance will be 50Ω for the lower 2/3 of the backplane which contains all the trigger data paths. This impedance matches the AMP connector impedance and the impedance of the individual boards. The wiring in this section is all point to point, making for a fairly straightforward transmission line. Terminations for these lines will be on the receiving cards. The multi-drop transmission line of the VME backplane in the upper 1/3 of the backplane will have an impedance of 100Ω – before holes and connectors are added. The effective impedance of this section will drop to a little less than 50Ω after connectors and trace stubs on the individual boards are taken into account.

The VME specification is written for crates containing no more than 21 cards. In addition, the specification requires that VME signal stubs on individual boards be no greater than 5.08cm in length. The present design for the trigger processor crates contains 20 cards with a VME interface. Reducing the VME interface from two connectors to one has increased the difficulty of staying within the 5.08cm requirement. Special care will be taken throughout the design process to stay within the VME standards.

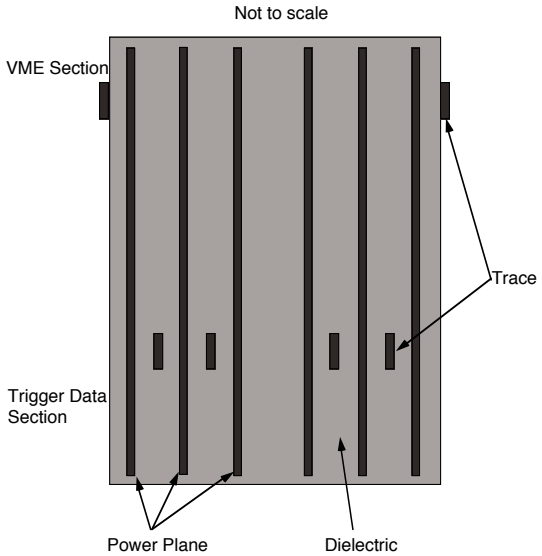

Figure 5. Schematic representation of backplane showing stack-up for VME and Trigger Data sections.

Preliminary calculations indicate it should be possible to route the high density wiring in the trigger data portion of the backplane in three signal layers. In order to ensure there are sufficient wiring channels and to maintain symmetry, four buried layers will be used in this section. A picture of the board stack-up is given in Figure 5. The organization of the layers is reflected about an extra thick core. An alternating power plane/signal plane structure produces a buried stripline design and surface micro-strip traces. The stripline structure provides good control over crosstalk and general noise immunity. The outside signal layers will be used mostly in the VME section of the backplane. Signal lines in that section will have ground traces running between each pair of lines to reduce crosstalk. Signals in the trigger data portion will be constrained, but not strictly limited to, the buried stripline layers.

2.2.4 Data Rates

All signals in the trigger data portion of the backplane will be transmitted at 160 MHz. This data rate was chosen because it offers the opportunity to compress the number of data lines on the backplane by a factor of four and because it should be realizable by available technology. More testing should be done, at these rates, to produce a design that maintains the necessary signal fidelity and clock to data skews.

All signals in this section, including clocks, are transmitted point to point. In the present design, all signals are differential. It may be that, with the stripline construction and the more than 160 backplane to board power connections afforded by the AMP stripline connectors, the data signals can be transmitted single-ended. The option to use single-ended transmission awaits the result of further testing and simulation.

3. Detector to Crate Mapping

A preliminary mapping of the calorimeter to the Level 1 regional trigger crates is presented here. Trigger tower geometry has yet to be optimized, and changes in the calorimeter tower layout will result in changes to this mapping. The efficiency with which crates are packed will also be affected by changes in the calorimeter design.

3.1 Eta - Phi Space

The current proposal is for trigger towers to have a size of .087 in both phi and eta for all phi between eta of 0.0 and 2.1. This granularity produces 72 towers in phi and 24 towers in eta for each half of the calorimeter. Between eta of 2.1 and 2.6 the tower size changes to .174 in eta, with the phi granularity unchanged. This produces another three towers in eta. Therefore, between eta of 0.0 and 2.6, there are 1944 Electromagnetic and Hadronic trigger towers in the half detector. The Very Forward Calorimeter will have 18 trigger towers in phi and 4 towers in eta for eta between 2.6 and 4.0. The last region,

between eta of 4.0 and 5.0 will be divided into 9 towers in phi and 1 tower in eta. The Electromagnetic and Hadronic towers are combined on the detector, in the region of 2.6 < eta ≤ 5.0, producing a single trigger tower for each pair. The grand total of trigger towers is 7938 for the full calorimeter.

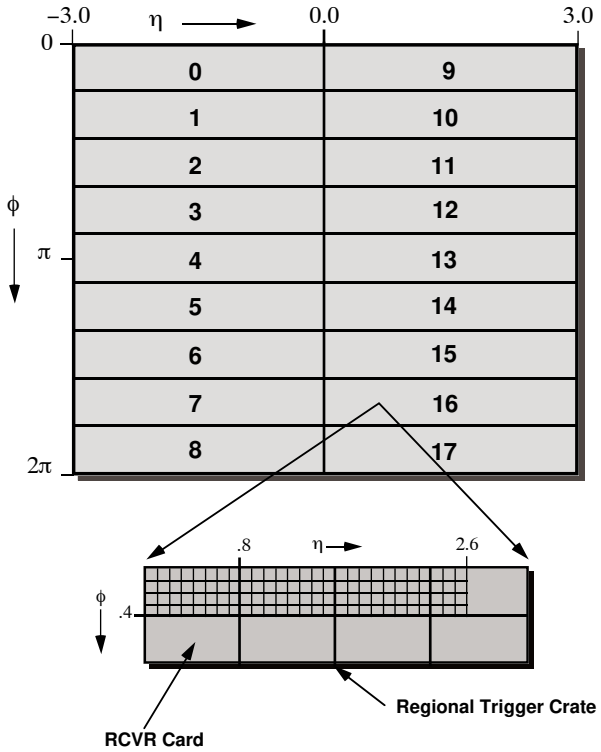

Figure 6. Mapping of Calorimeter Barrel and Endcap onto Trigger crates.

Figure 6 illustrates a mapping of the calorimeter onto the Regional Trigger Processor crates for the region between eta of -3.0 to 3.0. The 18 crates shown are required for the barrel and both endcaps. Another crate (not shown) is included for the Very Forward Calorimeter. Although this mapping does not completely minimize the intercrate cabling, it simplifies the backplane and produces a rack layout that minimizes the cable lengths between racks.

The Very Forward Calorimeter covers the region 3.0 < eta ≤ 5.0 and is not used for the isolated electron triggers. The electromagnetic and hadronic information is combined on the detector and sent to the trigger processing hardware as a single sum. This region can be covered with a single trigger crate by using the same input pins between the 8 bit electromagnetic data and 4 bit hadronic data inputs of the Electron Isolation card and the E_T inputs of the Jet Summary card. With this overlap, along with consistency in power/ground and clocking inputs, it is possible to substitute a Jet Summary card for an Electron Isolation card. The Jet Summary card forms the E_T sums and performs the trigger cuts on the data from up to eight sub-regions of the Very Forward Calorimeter.

3.2 Backplane Layout

The map of the calorimeter onto crates is used to derive a card to slot mapping within the crate itself. The layout of cards within the crate is setup to minimize the length of traces on the backplane. Figure 7 illustrates a layout which attempts to satisfy this condition. For reference the schematic mapping of the calorimeter onto a single crate is repeated with a slot numbering (left to right) superimposed on the eight Receiver cards. This numbering is relative within the trigger data region of the crate and is not meant to represent a specific card slot.

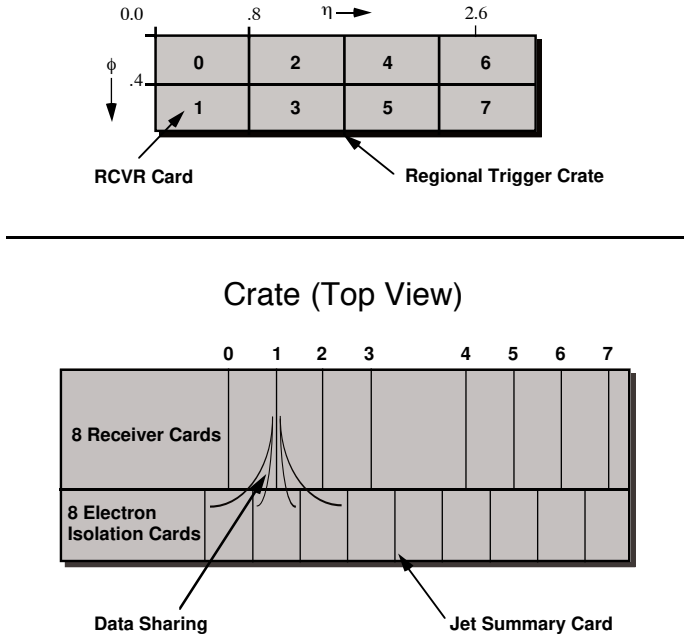

Figure 7. Card layout in the trigger data portion of the crate.

The sharing shown in the figure is representative of an "average" card and does not show the intercrate connections. Card 3, for instance, would share with cards 0, 1, 2, 4, and 5, within the crate, as well as with cards 0, 2, and 4 in the adjoining crate. Every card, except those at the extreme rim of the barrel, shares with eight other cards. The four "corner" neighboring cards only transmit 2 bits of hadronic information to central card.

4. Receiver Card

The Receiver card is the largest board in the crate. It is 9U by 400mm. Both sides of the card are fully utilized to receive and process calorimeter trigger data. The rear side of the card receives the calorimeter data from optical fibers, translates from fibre to copper, and converts from serial to parallel format. The leading edge of the board will provide strain relief and some space for a small coil of fiber. The front side of the card contains circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. There are also lookup tables and adder blocks on the

front. The lookup tables translate the incoming information to transverse energy on several scales. They are also used to test for Quiet and Minimum Ionization thresholds for each trigger tower. The memories were placed on this card, rather than the processing cards, because the sharing of data between processing cards would have required nearly twice as many memory chips. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for intercrate sharing.

4.1 Inputs

Each card is designed to receive 32 fibres from the FERMI [2] front-end readout system on the calorimeter. Each fibre transmits either two towers of hadronic or electromagnetic information per crossing. The data is transmitted on the fiber in a compressed eight bit format, providing a total of 16 data bits. The present design uses transmitter and receiver links capable of handling 21 bits of information in 25 nsec with a baud rate of 960 Mbaud. The additional 5 bits, not used for data, contain a single Hamming code generated from the 16 bits of data. This code is sufficient to detect all single and double bit errors as well as many multiple bit errors. The rear of the Receiver card, containing the fibre receiving circuitry is shown in Figure 8.

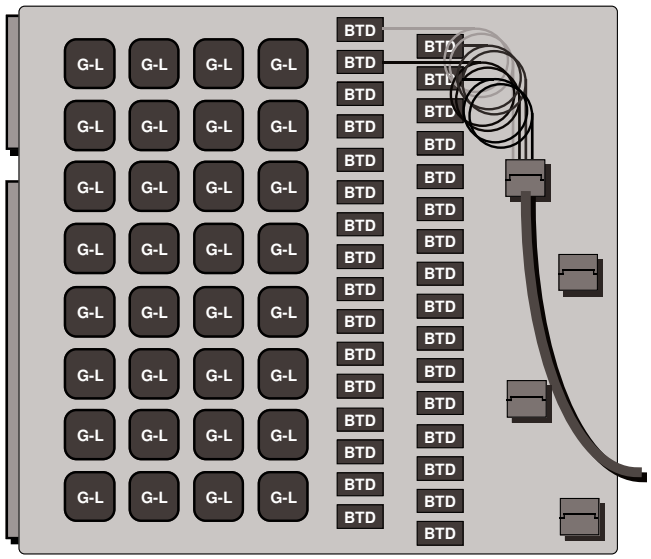

Figure 8. Rear view of the Receiver card and the fibre receiver circuitry.

The mapping presented in section 3.1 shows two Receiver cards in each crate that are not fully utilized. The first 12 towers connected to each of these two cards form a partially filled 4 x 4 region which includes separate electromagnetic information for electron isolation. The front end electronics, reading out the region between eta of 2.6 to 5.0, sums the electromagnetic and hadronic towers on the detector before sending the data to the Level 1 regional Trigger crates. The Endcap calorimeter ends at an eta of 3.0. With a

subdivision in phi of 18 we have a resolution, between eta of 2.6 to 3.0, equivalent to approximately one 4x4 sub-region for each phi division. We plan to complete the coverage of the Endcap calorimeter by including one tower ($2.6 < \text{eta} \leq 3.0$) in each of the partially filled Receiver cards. This uses a 13th input channel on the card. Whereas the other front end electronic channels transmit two towers of information per fibre per crossing, this channel must be limited to one tower per fibre in order to limit the data on the Receiver card to the usual two 4 x 4 regions transmitted to the Jet Summary card.

In order to minimize the cost of under-utilizing Receiver cards, those cards in the region of $2.6 < \text{eta} \leq 3.0$ will not have fibre receiving circuits and Synchronizing ASICs installed in the 19 unused channels. Since those circuits are likely to be the most expensive components on the board, partial assembly should achieve a major savings over the standard Receiver board cost.

The fibre optic link is also used to transmit synchronization information either on a regular basis or on demand. The re-synchronization philosophy will be discussed in greater detail in section 4.3.

4.2 Fibre Receiver

In the present design, the fibre receiver is made up of two separate components: The fibre to copper converter and the serial to parallel converter. As optical communication technology advances it is possible that integrated receivers (fibre to copper/serial to parallel), suitable to our application, will become available. For the present, we will concentrate on solutions that are available today in the market place and continue to examine any new offerings. The components used on the Receiver card will have to match those used on the calorimeter front end electronics to transmit the information.

Two separate fibre receivers have been considered for this design. The first device, made by BT&D, is one already in use at University of Wisconsin High Energy Physics. It is a high quality component in a 24 pin package, with long laser diode lifetime (transmitter), and a fiber pigtail. The pigtail is important in reducing the impact on the laser diode cavity by reflections from the first optical connection. This device is meant to operate at higher bandwidths and longer distances than we require and has a price of approximately $700(US) per end. BT&D have indicated they will produce a less expensive device aimed at a different market niche sometime in the future.

The second converter is a more recent offering by Finisar. It is designed to handle data rates over the range of 100 Mbaud to 1.5 Gbaud and drive fibre lengths up to 500 M. The device is powered by a single +5V supply and is packaged in a .9" by 2.5" by .5" high case. The long dimension includes the fibre connector. The output from the receiver is differential ECL, but not at

true ECL levels. Capacitve coupling to the serial to parallel converter is required. The lasing diode lifetime, at 210,000 hours, is about half that of the BT&D device, but without an understanding of the statistical distribution it is difficult to determine the impact this will have on a 4000 link system. The specifications list the Bit Error Rate (BER) of this receiver at $< 10^{-12}$ for an input dynamic range of -13 to +2 dBm. Finisar gives the typical value for the BER as $< 10^{-15}$. These BERs are evaluated using a 2^7 - 1 pseudo random bit sequence. The price for the Finisar device is presently $250(US)/pair in lots of 1000.

Any transmitter/receiver pair considered for this application should be tested to determine the extent to which fibre length, baud rate, or environmental conditions degrade the BER.

The second component of the receiver duo is the serial to parallel converter. For the present design we have considered the Hewlett Packard HDMP-1014. It has several advantages over other offerings. The receiver and transmitter are packaged separately in 80 pin surface mount quad packages. Separate packaging of the receiver/transmitter pair leads to correspondingly lower power consumption at each end, about 2 watts, and a more compact package. A pair can transmit and receive 21 bit data frames and does not require 8/10 encoding. A single bit control switches between command and data transmission "on the fly". This last feature is particularly important to the synchronization scheme we are proposing. Finally, the parallel outputs are true ECL levels, providing a good match to the high speed circuitry downstream from the receivers. These devices are presently priced at $100(US)/pair in lots of 1000.

The ground and power planes in the region of the fiber to copper converters will be split to minimize channel to channel crosstalk and will not be connected through the board to the digital power planes. We expect to use a separate voltage source for the optical converters. Filters will be used on the power inputs of the HP chips to reduce the possibility of coupling between the individual Phase Lock Loops. From a routing standpoint, there are few traces on the rear of the board up to the region containing the HP receivers. The outputs of the HP receivers will generate 32 x 21 lines of data. This set of lines will be referenced to the digital power planes and routed within them, in stripline fashion, to the Synchronization ASICs. Presently, the design has the fiber receivers at the back of the board (farthest from the backplane). We are exploring the interchange of positions of the HP converters and the fiber receivers to minimize the routing of the parallel outputs to the Synchronizers.

4.3 Synchronization

The synchronization circuitry is contained on the front side of the Receiver card along with the memory look up tables and adder tree. Figure 9 shows the organization of these components on the board. The outputs of the HP